WHAT IS CLAIMED IS

1. A scrambling system in multicarrier code division multiple access (MC-DCMA), comprising:

a transmitter for receiving a user's bit stream, using a fixed scrambling code which is predetermined according to the user's orthogonal code or a number of users, generating multicarrier signals, and outputting them; and

a receiver for using a scrambling code matched with the scrambling code used by the transmitter, and receiving the multicarrier signals from the transmitter.

2. The scrambling system of claim 1, wherein the scrambling code multiplied to each subcarrier by the transmitter uses a predetermined pattern established according to the user's orthogonal code combination and it is fixed while the identical user's orthogonal code combination is maintained.

3. The scrambling system of claim 1, wherein the transmitter comprises:

a symbol modulator for receiving a bit stream of a k-th user, and modulating the same according to a modulation method determined by the system;

a multiplier for multiplying respective modulation symbols modulated by the symbol modulator by an orthogonal code C_k having an N chip length, and spreading them into chip sequences;

an adder for adding the users' chip sequences spread by the multiplier in synchronization with symbol timing;

an interleaver for interleaving the chip sequences of M symbols added by the adder and arranging the chips belonging to an identical symbol by an M chip interval;

a serial/parallel converter for converting the chip sequences of the symbols arranged by the interleaver into parallel chip signals with a size identical to the number of subcarriers;

a scrambling chip vector generator for providing scrambling codes having a length identical with the number of subcarriers to the parallel chip signals of the serial/parallel converter, and multiplying them chip by chip;

an inverse fast Fourier transformer (IFFT) for performing inverse fast Fourier transform for the scrambled chip signals; and

a signal generator for generating baseband multicarrier signals from the outputs of the IFFT.

4. The scrambling system of claim 3, wherein the scrambling chip vector generator includes a multiplier for multiplying the parallel chip signals of the serial/parallel converter by the scrambling codes.

5. The scrambling system of claim 3, wherein the signal generator comprises:

a parallel/serial converter for converting the parallel chip signals converted by the IFFT into serial chip signals; and

a guard time inserter for inserting guard time into the serial chip signal converted by the parallel/serial converter.

6. The scrambling system of claim 1, wherein the scrambling code satisfies a condition for minimizing the PAPR performance measure, PAPRo which is defined according to the subsequent equation:

$$\Pr\left\{\frac{\max\limits_{0\le t<T_s}|y(t)|^2}{E(|y(t)|^2)} > PAPR_0\right\} = P_0$$

where y(t) is an output signal of the transmitter, T_s is a symbol period, and Po is the output signal clipping probability which is specified according to the system requirement.

7. The scrambling system of claim 1, wherein the transmitter finds a fixed scrambling pattern for maintaining the PAPR to be a minimum value for the current user's orthogonal code combinations, and uses the scrambling code while the user's orthogonal code combination is maintained.

8. The scrambling system of claim 7, wherein the fixed scrambling pattern is selected as a single scrambling pattern that has a value close to the PAPR caused by the scrambling patterns which are optimized at each code combination over all code combinations before operating the system.

9. A scrambling method in multicarrier code division multiple access (MC-CDMA), comprising:

(a) a transmitter receiving a user's bit stream, using a fixed scrambling code which is predetermined according to the user's orthogonal code or a number of users, generating multicarrier signals, and outputting them; and

(b) a receiver using a scrambling code matched with the scrambling code used by the transmitter in (a), and receiving the multicarrier signals from the transmitter.

10. The scrambling method of claim 9, wherein the scrambling code multiplied to each subcarrier in (a) uses a predetermined pattern established according to a current user's orthogonal code combination and it is fixed while the identical user's orthogonal code combination is maintained.

11. The scrambling method of claim 9, wherein (a) comprises:

(a-1) modulating bit streams of a k-th user into modulation symbols, multiplying the respective modulation symbols by an orthogonal code C_k, and spreading them into chip sequences;

(a-2) adding the users' chip sequences spread in (a-1) in synchronization with symbol timing, interleaving the chip sequences of M symbols that will be transmitted in parallel, and arranging the chips belonging to an identical symbol by an M chip interval; and

(a-3) converting the chip sequences arranged in (a-2) into parallel chip signals having a number of subcarriers, multiplying the parallel chip signals by the scrambling code, modulating each chip for each subcarrier through inverse fast Fourier transform, and generating and outputting multicarrier signals.

12. The scrambling method of claim 11, wherein the generation of the multicarrier signals in (a-3) comprises multiplying the scrambling codes by the parallel chip signals input for inverse fast Fourier transform for each chip.

13. The scrambling method of claim 9, wherein the scrambling code satisfies a condition for minimizing the PAPR performance measure, PAPRo which is defined according to the subsequent equation:

$$\Pr\left\{\frac{\max\limits_{0\le t<T_s}|y(t)|^2}{E(|y(t)|^2)} > PAPR_0\right\} = P_0$$

where y(t) is an output signal of the transmitter, T_s is a symbol, and Po is the output signal clipping probability which is specified according to the system requirement.

14. The scrambling method of claim 9, wherein the transmitter finds a fixed scrambling pattern for maintaining the PAPR to be a minimum value for the user's orthogonal code combinations, and uses the scrambling code while the user's orthogonal code combination is maintained.

15. The scrambling method of claim 14, wherein the fixed scrambling pattern is selected as a single scrambling pattern that has a value close to the PAPR caused by the scrambling patterns which are respectively optimized at each code combination over all code combinations before operating the system.

16. A recording medium storing a program comprising:

(a) modulating bit streams of a k-th user into modulation symbols, multiplying the respective modulation symbols by an orthogonal code C_k, and spreading them into chip sequences;

(b) adding the users' chip sequences spread in (a) in synchronization with symbol timing, interleaving the chip sequences of M symbols that will be transmitted in parallel, and arranging the chips belonging to an identical symbol by an M chip interval; and

(c) converting the chip sequences arranged in (b) into parallel chip signals, multiplying the parallel chip signals by the scrambling code, modulating each chip for each subcarrier through inverse fast Fourier transform, and generating and outputting multicarrier signals.